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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,099	10/08/2003	Tzyy Haw Tan	P-6122-US	4462

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EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 01/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/680,099	TAN ET AL.	
	Examiner	Art Unit	
	Luan Thai	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 08 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 6-7, 12, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198) and Chen et al. (6,448,110), and under U.S.C. 102(e) as being anticipated by Corisis (6,607,937), separately.

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 6-7, 12, 14, and 16, Chia et al. (see specifically figures 2-3) disclose a semiconductor package comprising: a semiconductor chip (110) having plurality of electrode pads on its active surface, plurality of solder balls (180-182) at an underside of the package, external leads (143) of Gull-wing type at a side edge of the package, and a printed circuit board (196) having plurality of pads (192) soldered to solder balls (180-182) of the package and plurality of pads (190) soldered to external leads (143) of the package.

Similarly, Lin (figures 1 and 3) discloses a semiconductor package (10) comprising: a semiconductor chip (14) having plurality of electrode pads (18-20-21) on its active surface, plurality of solder balls (12) at an underside of the package, external leads (38) of Gull-wing type at a side edge of the package, and a printed circuit board (64) having plurality of pads (66) soldered to solder balls (12) of the package and plurality of pads (66) soldered to external leads (38) of the package.

Lin et al. (see specifically figures 4-5) disclose a semiconductor package (52) comprising: a semiconductor chip (20) having plurality of electrode pads on its active surface, plurality of solder balls (32) at an underside of the package, external leads (36) of Gull-wing type at a side edge of the package, and a printed circuit board (38) having plurality of pads (40) soldered to solder balls (32) of the package and plurality of pads (40) soldered to external leads (36) of the package.

Chen et al. (see specifically figure 4) disclose a semiconductor package (100) comprising: a semiconductor chip (66/70), plurality of solder balls (74) at an underside of the package, external leads (80) of Gull-wing type at a side edge of the package, and a printed circuit board (102), and plurality of pads inherently formed thereon for soldered to solder balls (74) and external leads (80) of the package (100).

Also, Corisis (figure 5) discloses a semiconductor package comprising: a semiconductor chip (424) having plurality of electrode pads on its active surface, plurality of solder balls (443a) at an underside of the package, external leads (443b) of Gull-wing type at a side edge of the package, and a printed circuit board (430) having

plurality of pads (431a) soldered to solder balls (443a) of the package and plurality of pads (431b) soldered to external leads (443b) of the package.

3. Claims 1, 3, 6-10, and 12, are rejected under 35 U.S.C. 102(b) as being anticipated by Chillara et al. (5,648,679).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 6-10, and 12, Chillara et al. (see specifically figures 4-6) disclose a semiconductor package (120) comprising: a semiconductor chip (132) having an active surface having a plurality of bonding pads (134-136) from which bonding wires (138-140-150-154) bonded (see figure 4A), wherein at least pad (136A), pad (136B), and pad (134A) are ground terminal, power supply terminal, and signal terminal, respectively, of the circuitry of the semiconductor chip (132). Chillara et al. further disclose plurality of solder balls (129) at an underside of the package, external leads (130) of Gull-wing type at a side edge of the package.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 4, 11, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), Chen et al. (6,448,110), and Corisis (6,607,937), in view of Nguyen et al. (6,707,140).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 2, 4, 11, 13, and 15, each of Chia et al., Lin, Lin et al., Chen et al., and Corisis discloses the claimed invention, including the external leads being surface mounted leads of type Gull-wing, as detailed above except for other type of the external leads (e.g., J-lead or through-hole lead).

External leads of type J-lead or through-hole lead, however, is commonly applied in the art, especially in lead frame art, as taught by Nguyen et al. (figures 10-11-12-13). Nguyen et al. disclose the external leads of a package can be a surface mount lead of: type J-lead (figures 10-11), type Gull-wing (figure 12), or type through-hole lead (figure 13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the external leads of the package of Chia et al., Lin, Lin et al., or Corisis, by using type J-lead or through-hole lead as taught by Nguyen et al., since such types of leads are conventionally applied in the art, as disclosed by Nguyen et al., and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), and Corisis (6,607,937).

Regarding claim, each of Chia et al., Lin, Lin et al., and Corisis disclose the claimed invention, including the external leads being soldered to the printed circuit board, as detailed above, except for teaching the external lead being absorb part of a strain

between the package and the printed circuit board when the external lead is soldered to the printed circuit board.

Since external leads being soldered to the printed circuit board is disclosed by Chia et al., Lin, Lin et al., and Corisis, and it would have been obvious that a part of strain (e.g., thermal strain, mechanical strain, and thermo mechanical strain) must be exist and absorbed by the external leads.

7. Claims 4, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), and Corisis (6,607,937), in view of Weeks (5,242,100).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 4, 13, 15 and 17, each of Chia et al., Lin, Lin et al., and Corisis disclose the claimed invention, including the external leads being surface mounted leads of type Gull-wing, as detailed above except for other type of the external leads (e.g., through-hole lead).

External leads of type through-hole lead, however, are commonly applied in the art, especially in lead frame art, as taught by Weeks (figures 4-5). Weeks discloses the external leads (62) of a package (60) can be a surface mount lead of: type Gull-wing (figure 3) or type through-hole lead (figure 5), wherein through-hole leads are inserted into the holes of the pads (41-53) formed on the printed circuit board (40) (see figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Chia et al., Lin, Lin et al., or Corisis, by applying

through-hole leads for the package, since such through-hole leads are conventionally applied in the art, as disclosed by Weeks, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

8. Claims 18, 20, 22-23, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), Chen et al. (6,448,110), and Corisis (6,607,937), in view of Ito et al. (6,064,179).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 18, 20, 22-23, 25 and 27, each of Chia et al., Lin, Lin et al., Chen et al., and Corisis discloses the claimed invention as detailed above except for the circuit board having a voltage monitor installed thereon, and the package being used in a computer having an audio input device.

Ito et al. teach a computer (see figure 5) comprising at least a mother circuit board (33) having a voltage monitor and a plurality of package electrically connected thereon (Col. 9, lines 12+), wherein the computer inherently having an audio input device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the external terminal structure of the semiconductor package as disclosed by Chia et al., Lin, Lin et al., Chen et al., and Corisis to Ito et al. computer since such application is held to be within the ordinary designing ability expected of a person skilled in the art.

9. Claims 19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), Chen et al. (6,448,110), and Corisis (6,607,937), in view of Ito et al. (6,064,179) and further in view of Nguyen et al. (6,707,140).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 19 and 24, the proposed package of Chia et al., Lin, Lin et al., Chen et al., and Corisis discloses the claimed invention, including the external leads being surface mounted leads of type Gull-wing, as detailed above except for other type of the external leads (e.g., J-lead).

External leads of type J-lead, however, are commonly applied in the art, especially in lead frame package art, as taught by Nguyen et al. (figures 10-11-12). Nguyen et al. disclose the external leads of a package can be a surface mount lead of: type J-lead (figures 10-11) or type Gull-wing (figure 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the external leads of the proposed package of Chia et al., Lin, Lin et al., Chen et al. and Corisis, by using type J-lead as taught by Nguyen et al., since such types of leads are conventionally applied in the art, as disclosed by Nguyen et al., and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

10. Claims 21 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over each of Chia et al. (5,563,446), Lin (5,508,556), Lin et al. (5,239,198), Chen et al. (6,448,110), and Corisis (6,607,937), in view of Ito et al. (6,064,179) and further in view of Weeks (5,242,100).

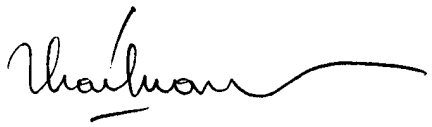
Regarding claims 21 and 26, the proposed package of Chia et al., Lin, Lin et al., Chen et al. and Corisis discloses the claimed invention, including the external leads being surface mounted leads of type Gull-wing, as detailed above except for other type of the external leads (e.g., through-hole lead).

External leads of type through-hole lead, however, are commonly applied in the art, especially in lead frame package art, as taught by Weeks (figures 4-5). Weeks discloses the external leads (62) of a package (60) can be a surface mount lead of: type Gull-wing (figure 3) or type through-hole lead (figure 5), wherein through-hole leads are inserted into the holes of the pads (41-53) formed on the printed circuit board (40) (see figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed package of Chia et al., Lin, Lin et al., Chen et al. and Corisis, by using through-hole leads, since such through-hole leads are conventionally applied in the art, as disclosed by Weeks, and such modification is held to be within the ordinary designing ability expected of a person skilled in the art.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:45 AM - 4:15 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Luan Thai
Primary Examiner
Art Unit 2829
January 13, 2005